DETAILED DESCRIPTION

As disclosed herein, the present invention describes a novel method and system for determining PN phase in a spread spectrum communications system.

Referring to Fig. 8, there is shown a pictorial diagram of a telecommunications system incorporating features of the present invention. Although the present invention will be described with reference to the embodiment shown in the drawings, it should be understood that the present invention might be embodied in many alternate forms of embodiments, e.g., point-to-point duplex links or point-to-multipoint links. In addition, it should be understood that the teachings herein may apply to any group or assembly of hybrid TDMA-SS receivers, including those that are fixed in place; vehicle mounted; and/or hand carried. As will be made clear, the invention includes waveform structure, link maintenance, and rapid acquisition.

Still referring to Fig. 8, there is shown a full-duplex system 10 that is suitable for practicing this invention. Specifically, the system 10 employs direct sequence spread spectrum based techniques over an air link to provide data transfer between HUB 12 and a SPOKE 14. It will be appreciated that there may be more than one Spoke. The forward link (FL) from HUB 12 to SPOKE 14 contains a spread spectrum waveform that is constructed in the manner described herein, with the PN code being composed of relatively prime even-length and/or maximal length codes. In a similar manner, the return link

(RL) from SPOKE 14 to HUB 12 contains a spread spectrum waveform that is similar, or identical, to that of the FL.

Still referring to Fig. 8, HUB 12 includes a Spread Spectrum Modulator (SSM) 12b; the SSM 12b generates a desired spread spectrum waveform at a desired RF frequency. The SSM 12b also provides a Tx clock 12d that is used to clock the Tx Data 12e into the SSM 12b. The SSM 12b then combines the Tx data 12e with a spread spectrum PN code to produce the desired spread spectrum waveform. HUB 12 also includes an antenna 12a, which may transmit at any suitable RF frequency.

The signal generated by HUB 12 and transmitted by antenna 12a via the FL is received by SPOKE 14 via antenna 14a. Spoke 14 includes a spread spectrum correlator 14c1, PN generator 14c2, clock generator 14c3, and spread spectrum demodulator (SSD) 14c4. The received signal is then demodulated by SSD 14c4 and PN phase is maintained in accordance with features of the present invention described herein. It will be appreciated that all or partial demodulation functions may be contained within an integrated circuit (IC) such as a Field Programmable Gate Array (FPGA). Once the signal is acquired and the SPOKE 14 is tracking the received signal, the Rx Clock 14g and Rx Data 14f are output to the intended receiver circuitry. It

will be appreciated that the clocks 14g and 12d are synchronous and may be commanded to change frequency to correspond with PN code epochs as will be described herein; thus advantageously providing means to vary the data rate without interruption; and without the need for conventional bit synchronizers with associated synchronization time.

Similarly, SPOKE 14 generates a Tx Clock 14d and Tx Data 14e using the Spread Spectrum Modulator 14b in a similar fashion described earlier for a HUB. Likewise, HUB 12 may receive the RL signal via antenna 12a, and demodulate and track the signal as described earlier with receiver 12c to provide Rx Data 12f and Rx Clock 12g to the intended user.

Referring also to Figure 1, a Direct Sequence Spread Spectrum (DSSS) PN (pseudo noise) code, constructed of relatively prime component codes in accordance with the teachings of the present invention, repeats itself only once per major epoch (convention typically acknowledges the all 1's state of all component codes as the composite code's major epoch). It will be appreciated that longer PN codes (on the order of weeks, years, and decades) and composite PN code phase manipulations are more complex (Smart, data-aided acquisition; GPS-aided

acquisition; track-code acquisition; et cetera), and require near-real-time confirmation of PN composite code phase.

RELATIVE PRIMENESS

Relatively prime component codes constructed in accordance with features of the present invention do not share multiplicands of their code lengths. As an example, a PN code may be comprised of three component codes: X, Y, and Z. The length of X is 12 chips (2 x 2 x 3 are the multiplicands of 12). The length of Y is 315 chips (5 x 7 x 9), and the length of the Z component code is 601, a prime number. Although the component code lengths of 12 and 315 are not prime, they are relatively prime in that they do not share multiplicands. It will be appreciated that any suitable number of relatively prime component codes may be used.

XY AND XZ EPOCH SEPARATION

In accordance with features of the present invention, PN composite code phase is determined by XY and XZ epoch separation, independent of order of arrival, and relative (X-epoch) separation, independent of XY/XZ epoch contiguousness. Referring still to Figure 1 and also Figure 2, the PN code depicted in **Error! Reference source not found.** is representative of relatively prime codes. The X, Y, and Z

component codes lengths are 3, 7, and 23, respectively. X, XY, XZ, and XYZ epochs are depicted according to the legend shown in Figure 2. Still referring to **Error! Reference source not found.**, a unique event occurs at chip 210: an XY epoch follows an XZ epoch by a single X epoch. It will be appreciated that this positional relationship and 1 X-epoch separation occurs nowhere else within this PN code sequence constructed in accordance with the teachings of the present invention. At chips 273 and 276, another XY-XZ separation of a single X epoch is again found, but in this case, the XZ follows the XY epoch by one X epoch. At the 10^{th} XY-epoch (N_{xy}) number of chips (10 x 7 x 3 = 210 chips), XY epochs have a phase of zero chips and XZ epochs have a phase of 3 chips, which is 1 X epoch. Once the position of XZ/XY-separated-by-one-X-epoch is discovered as described herein, then everything about the PN code is known relative to PN code phase.

DETERMINING THE XZ-XY COMPOSITE CODE PHASE POSITION

The phase position at which an XZ epoch precedes an XY epoch by one X epoch is determined as described herein. The search is performed using modulo arithmetic, as shown in Equation 1. The N_{xy} epoch is discovered by incrementing N_{xy} of Equation 1. Equation 1 searches the PN code at XY epoch number of chips

to see if this XY epoch number of chips is an XZ number of chips plus one X epoch.

$$(N_{XY} \times L_X \times L_Y) MOD(L_X \times L_Z) = L_X \quad \text{Equation 1}$$

It can be seen that the length of the X code, L_X, is found in all three terms of Equation 1. By eliminating this term from Equation 1, a simplification results and smaller numbers can be used, as shown in Equation 2. This improvement is significant when long code lengths are involved and very large numbers must be handled.

$$(N_{XY} \times L_Y) MOD(L_Z) = 1 \quad \text{Equation 2}$$

Referring to Equation 2 and Figure 3, it can be seen in Figure 3 at chip 70, the 10^{th} Y epoch, that a Z epoch occurs at chip 69. In other words, at the 10^{th} Y-epoch number of chips, the PN code has a Z epoch number of chips plus 1 chip, which is the exact relationship being sought. Note that this same relationship occurs L_Z (which is 3) times in this example at every L_Y number of Y epochs. The same relationship occurs 23 Y epochs later at chip 231 and 23 Y epochs after that at chip 392. Equation 2 finds the first relationship at chip 70, the 10^{th} Y epoch.

This scaling effect can also be seen in Figure 4. It will be appreciated that the difference between Figure 1 and Figure 4

is that the X component code length of Figure 4 is 2 chips, as compared to the 3 chip length of the X code in **Error! Reference source not found.**. It can be seen that the XY epochs and XZ epochs are separated by the identical number of X epochs in the two figures; the figures are scaled by the length of the X code.

NORMALIZED, EPOCH, AUTONOMOUS PHASE NUMBERS

Equation 2 identifies the 10^{th} XY epoch as the epoch at which an XZ and an XY are separated by one X epoch, in that order of arrival, which is referred to as N_{xy}. An XY epoch is 21 chips long (the length of the X code times the length of the Y code, in this example). Therefore, 10 XY epochs is 210 chips in length. Now that the number of chips is known at which XZ and XY epochs have a phase relationship of one X epoch, the composite code phase position can be known where XZ and XY epochs are separated by n X epochs. As an example, an XZ epoch should precede an XY epoch by 2 X epochs at chips 2 x 210 = 420 in the example PN code of **Error! Reference source not found.**. It can be seen that the XY epoch at chip 420 is preceded 2 X epochs by an XZ epoch. An XZ epoch precedes an XY epoch by 22 X epochs at 22 N_{xy} number of chips (22 x 210 MOD 483 = 273); the XZ epoch at chip 207 is 22 X epochs before the

XY epoch at chip 273. N_{xy} is normalized to 1 X-epoch separation of an XZ and XY epoch. Normalizing this relationship to a separation of 1 X epoch, the PN composite code phase at the XY epoch of any XZ to XY separation can be determined in accordance with features of the present invention.

It will be appreciated that XZ epochs have a phase of 1 (X epoch) at the NEAP epoch of the third component code; the third component code (Y) has zero phase at the NEAPth XY epoch; the NEAP number is not affected by a non-zero phase of the third component code.

Referring to Figure 5, there is shown a flow chart showing one method for determining the PN composite code phase of the XY epoch given any XY to XZ separation: it can be seen from Figure 5 that PN composite code phase can be determined regardless of the order of XY and XZ epoch arrival. Further, XY and XZ epochs do not have to be contiguous. Referring also to Figure 6A, NEAP counters and latches are depicted in the block diagram. The X-epoch counters 6A1 and 6A2, are latched on XY and XZ epochs, respectively. If the XY-latched X epoch is greater than the XZ-epoch latched X epoch, the XY epoch has occurred after the XZ epoch, and ΔX is positive.

A function of the X-epoch counters 6A1,6A2 is to latch the X-epoch count at the most recent XY and XZ epochs. However, should an event occur that precludes the X-epoch latch at the most recent XY or XZ, subsequent XY or XZ epochs can latch the X-epoch counter to satisfy the NEAP feature of the present invention. It can be seen in the flowchart of Figure 5 that ΔX modulo the length of the Z code is employed to keep the value of ΔX smaller than the length of the Z code in order to keep numbers as small as possible when calculations are made (steps 53 and 54). It should be noted that the XY/XZ-latched X-epoch counters 6A1, 6A2 are self-correcting; if a counting or latch error is made, the error is corrected at the next XY or XZ-latched X-epoch count because only the difference between the two latched values is important. When an error is introduced into each of the latched terms, the difference factors out the error.

Still referring to Figure 5, when ΔX is positive, step 52, the PN composite code phase at the last-latched XY epoch is calculated as shown in Figure 5, step 53 and Equation 3. Equations may be derived to calculate the PN composite code phase at the last-latched XZ epoch, but given that the length of the Y code is shorter than the length of the Z code, XY

epochs are more numerous and occur more often than XZ epochs, and calculation of the PN composite code phase at the last-latched XY epoch is the preferred embodiment of the NEAP feature of the present invention. According to Equation 3, the PN composite code phase at the last-latched XY epoch is the NEAP XY epoch, calculated according to Equation 2, times the length of an XY epoch times the XZ/XY separation. This result, which may be a number of chips longer than the length of the PN code, modulo the length of the PN code (the length of the X code times the length of the Y code times the length of the Z code) provides a phase number of chips less than the length of the PN code.

$$\theta_{XY} = \left[N_{XY} \times L_X \times L_Y \times \left(\Delta X \, MOD \, L_Z\right)\right] MOD \, L_{XYZ} \quad \text{Equation 3}$$

If the last-latched epoch is an XZ epoch, ΔX is negative, and the PN composite code phase at the last-latched XY epoch is calculated according to step 54 and Equation 4. There is only a Z number of XY epochs in a PN code. Therefore, when ΔX is negative, its absolute value is subtracted from the length of the Z code, and the PN composite code phase is calculated as otherwise for the positive ΔX case.

$$\theta_{XY} = \left[N_{XY} \times L_X \times L_Y \times \left(L_Z - \left(\left|\Delta X\right| MOD \, L_Z\right)\right)\right] MOD \, L_{XYZ} \quad \text{Equation 4}$$

Equations and flowcharts up to this point have referenced PN codes composed of three component codes. The methods and system presented in this document are not limited to PN codes composed of 3 component codes and can be applied to PN codes composed of any suitable number of PN component codes.

NEAP FEATURE OF THE PRESENT INVENTION CORRECTIVE ACTION

Once the NEAP feature of the present invention has detected a PN composite code phase error, corrective action can be taken as shown in Figures 6B, and 7.

The assumed PN composite code phase at an XY epoch (θ_{PNXY}) is equal to the number of sampling clocks actually counted and latched at the XY epoch ($\#SCLK_{XY \rightarrow ChipX}$) plus the number of chips intentionally slipped or advanced ($\Delta\theta_{XY}$), step 72. The smallest unit of a PN code is a chip, and the master (sampling) clock can equal the chipping rate, or it can be an integer multiple of the chipping rate.

Supporting data-aided PN code acquisition, the assumed PN composite code phase ($\theta_{PN\ @\ TSI\ clock}$) at the desired granularity of the Time Since Initialization counter (a counter that counts cycles of the master oscillator used as the master clock, which is shown as an example 10 MHz in Figure 6B is equal to the value of the TSI counter at the precision of the

desired granularity converted to chips ($TSI_{tick \rightarrow chips}$) plus intentional PN code slips and advances ($\Delta\theta_{XYZ}$) plus accumulated phase ($\Delta\Sigma\theta$, which is the accumulated phase variation from the nominal chipping rate, the difference between the actual number of chips generated in a time period and that very time period measured by the master clock, converted into chips by an exact time-to-chip relationship). This relationship, PN composite code phase at a TSI tick, is expressed in Equation 5. The relationship between the sampling clock count latched by a TSI tick and the TSI counter is expressed in Equation 6.

$$\theta_{PN@TSI\ tick} = TSI_{tick \rightarrow chips} + \Delta\theta_{XYZ} + \Delta\Sigma\theta \quad \text{Equation 5}$$

$$\#SCLK_{TSI\ tick \rightarrow chips} = TSI_{tick \rightarrow chips} + \Delta\Sigma\theta \quad \text{Equation 6}$$

If the TSI-tick-latched sampling clock counter 6B3 and the XY-epoch-latched sampling clock counter 6B2 are counting properly, the TSI-tick-latched counter 6B3 can be trusted to calculate accumulated phase by means of Equation 6. It is expected that PN phase errors will not originate from the counters 6B3, 6B2 and clock counter 6B1 shown in Figure 6B. However, the counters can be verified by multiplexing the latches shown in Figure 6 with a latch from a processor. The processor can latch both counters (6B2 and 6B3) and verify that they have the same count. If the TSI counter 6B1 has made

a mistake, the correction will be made in the calculation of accumulated phase, $\Delta\Sigma\theta$, by means of Equation 6 (step 74). All other phase errors, determined by step 73, are corrected by means of an unintentional slip calculation, shown in Figure 7, step 74, which is added to the value of the aggregate intentional slip, and the sum becomes the new bookkeeping value of intentional slips ($\Delta\theta_{XYZ}$). Advantageously, features of the present invention detect the phase error, if any, and makes required corrections, leaving the process transparent to the communication network.

It will be further appreciated that the invention described herein advantageously accomplishes PN composite code phase determined substantially precisely by XY and XZ epoch arrivals and relative (X-epoch) separation. The NEAP feature of the present invention operates independently of XY/XZ epoch contiguousness and order of arrival (see Figures 5 and 6A). Once a PN code phase error is detected, the needed correction is made, preserving the communication network from interruption in a manner that is transparent to the communication network.

It will be appreciated that the present invention advantageously provides a system and method where PN composite

code phase can be known precisely by XY and XZ epoch arrivals, and relative (X-epoch) separation.

It should be understood that the foregoing description is only illustrative of the invention. Various alternatives and modifications can be devised by those skilled in the art without departing from the invention. For example, Equation 1 may be modified such that:

$$\left(N_{MAX} \times L_X \times L_Y\right) \; MOD \; \left(L_X \times L_Z\right) = L_X M \quad \text{Equation 7A}$$

Where M is an integer 1,2, 3,…

It will be appreciated that once Nxy is determined in accordance with features of the present invention then all M * X-Epoch separations of XY and XZ epochs are known.

It will be further appreciated that any suitable method for combining component codes and generating local epoch symmetrical composite PN codes may be used. It will be further appreciated that in embodiments using more than three component codes; for example, four component codes; the component codes (X, Y, Z1, and Z2) may be MAND combined X⊕(Y•(Z1⊕Z2)), meaning X xor Y AND Z1 xor Z2, (where AND refers to AND-Boolean logic). In the preferred embodiment, one of the PN codes to the left of the AND in the MAND code is assigned to be an even-length code with special auto correlation properties. In alternate embodiments, any of component codes could be assigned to be a suitable length with suitable autocorrelation properties. In addition, a MAND composite code composed of four component codes in accordance with the teachings of the invention has partial correlation

properties with its X, Y, and/ or (Z1⊕Z2) component codes. For example, when a MAND code ,where a MAND code is defined for a three component code which has been logically combined according to X xor (Y and Z), or a four component code has been logically combined according to X xor (Y and (Z1 xor Z2)), is mixed (or correlated) by the receiver with an exact copy of its X code, and the X code is aligned (in phase) with the MAND code, the MAND PN encoded data is recovered, albeit the recovered signal has ¼ the power than if full correlation were achieved. Thus, by acquiring, in accordance with the teachings of the invention, an even-length code first, symbol synchronization [of even or odd length] can be achieved independent of symbol synchronizers, and a partial correlation allows the recovery of encoded or unencoded data from the received signal. It will be further appreciated that in 4-component code systems the components may be MAJ combined codes ,where a MAJ combined code is defined for a three component code which has been logically combined according to (X and Y) xor (X and Z) xor (Y and Z). MAJ for a 4-component-code sequence:

X, Y, Z1, AND Z2: $MAJ = (X \bullet Y) \oplus (X \bullet Z1) \oplus (X \bullet Z2) \oplus (Y \bullet Z1) \oplus (Y \bullet Z2) \oplus (Z1 \bullet Z2)$

It should be understood that the foregoing description is only illustrative of the invention. Thus, various alternatives and modifications can be devised by those skilled in the art without departing from the invention. For example, MOD combinatorial logic, e.g., X ⊕ Y ⊕ Z or X ⊕ Y ⊕ Z1 ⊕ Z2 may be used. Accordingly, the present invention is intended to

embrace all such alternatives, modifications and variances that fall within the scope of the appended claims.

It will be further appreciated that the aforementioned IC may be an application specific IC (ASIC), or a function of firmware. A suitable programming language such as a Very High Speed Integrated Circuit (VHSIC) Hardware Description (VHDL) Language file may define the operation of the ICs or firmware.